AMENDMENTS TO THE SPECIFICATION

Please amend the Specification as follows:

On page 1, before the first line, please insert:

--This application is a division of co-pending application number 10/015,434, filed December 13, 2001 which is a division of serial number 09/146,263, now U.S. Patent No. 6,350,706, issued February 26, 2002.--

On page 2, from line 23 to page 8, line 8:

In one embodiment, the present invention is a process for using a photo-definable layer in a ~~negative~~ positive mask scheme to manufacture a semiconductor device. This process may include forming a photo-definable layer that is convertible to an insulative material, exposing selected portions of the photo-definable layer to electro-magnetic radiation in a ~~negative~~ positive pattern scheme to convert the selected portions to an insulative material, removing exposed portions of the photo-definable layer, and using the non-exposed portions of the photo-definable layer as a patterned mask for further processing steps. In a further embodiment, the present invention is a semiconductor device including a substrate and at least one feature formed on the substrate by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a ~~negative~~ positive mask scheme and by using non-exposed portions of the photo-definable layer as a mask to form the one feature.

In another embodiment, the present invention is a process for etching an insulative layer using a photo-definable layer in a ~~negative~~ positive mask scheme. This process may include forming a photo-definable layer that is convertible to an insulative material, exposing selected portions of the photo-definable layer to electro-magnetic radiation in a ~~negative~~ positive pattern scheme to convert the selected portions to an insulative material, and removing exposed portions of the photo-definable layer and underlying portions of an insulative layer with a single-step etch

process. In a further embodiment, the present invention is a patterned insulative structure within a semiconductor device including a substrate and a patterned insulative layer formed on the substrate by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a ~~negative~~ positive mask scheme and by using non-exposed portions of the photo-definable layer as a mask to form the patterned insulative layer.

In another embodiment, the present invention is a process for etching an insulative layer followed by a conductive layer in the manufacture of a semiconductor device. This process may include forming an insulative layer over a conductive layer on a substrate, forming a photo-definable layer that is convertible to an insulative material, exposing selected portions of the photo-definable layer to electro-magnetic radiation to convert the selected portions to an insulative material, removing exposed portions of the photo-definable layer and underlying portions of the insulative layer with a single-step etch process to form a void within the insulative layer, and removing a portion of the conductive layer within the void. In further embodiment, the present invention is a conductive interconnect structure within a semiconductor device including a substrate, a first conductive layer over the substrate, and an insulative layer over the conductive layer. This structure may further include a second conductive layer formed within a desired portion of the insulative layer to create a conductive interconnect structure connected to the first conductive layer. This second conductive layer may be formed by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a ~~negative~~ positive mask scheme, by using non-exposed portions of the photo-definable layer as a mask to form a pattern within the insulative layer, and by using non-exposed portions of the photo-definable layer as a sacrificial mask in etching the second conductive layer.

In yet another embodiment, the present invention is a process for using a photo-definable layer to underlie an organic photoresist layer during the manufacture of an integrated circuit structure is provided. This process may include forming a photo-definable layer that is

convertible to an insulative material, creating a patterned organic photoresist layer over the photo-definable layer to leave unmasked portions of the photo-definable layer, exposing selected portions of the photo-definable layer to electro-magnetic radiation to convert the selected portions to an insulative material, and removing exposed portions of the photo-definable layer and underlying portions of the insulative layer with an etch process to form a void within the insulative layer. In a further embodiment, the present invention is a patterned insulative structure including a substrate and an insulative layer on the substrate formed by covering a photo-definable layer with a patterned organic photoresist, by converting unmasked portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a ~~negative~~ positive mask scheme, and by using non-exposed portions of the photo-definable layer and the organic photoresist as a mask to form a pattern within the insulative layer.

In a still further embodiment, the present invention is a process for using a photo-definable layer including forming a photo-definable layer that is convertible to an insulative material, exposing selected portions of said photo-definable layer to electro-magnetic radiation in a ~~positive~~ negative pattern scheme to convert the selected portions to an insulative material, removing non-exposed portions of the photo-definable layer with an etch process, using the ~~non-exposed~~ exposed portions of the photo-definable layer as a patterned mask for further processing steps, and leaving the exposed portions of the photo-definable layer as an insulative layer within the device. In a further embodiment, the present invention is a semiconductor device including a substrate and at least one feature formed on the substrate by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a negative mask scheme, by using exposed portions of the photo-definable layer as a mask to form at least one feature, and by leaving the exposed portions of the photo-definable layer on the substrate as an insulative layer.

In another embodiment, the present invention is a process for forming a self-aligned contact during the manufacture of a semiconductor device using a photo-definable layer in a positive mask scheme. This process may include forming an insulative layer over a substrate

having at least two spaced structures, forming over the insulative layer a photo-definable layer that is convertible to an insulative material, exposing selected portions of the photo-definable layer to electro-magnetic radiation in a ~~positive~~ negative pattern scheme to convert the selected portions to an insulative material, and removing non-exposed portions of the photo-definable layer with an etch process to expose selected portions of the insulative layer between the spaced structures. The process may also include removing the selected portions of the insulative layer to expose underlying portions of the substrate and depositing conductive material to form a self-aligned contact between the spaced structures. In a further embodiment, the present invention may be a self-aligned contact structure within a semiconductor device formed using a photo-definable layer in a ~~positive~~ negative mask scheme. This structure may include a substrate, an insulative layer formed on the substrate, and at least one self-aligned contact formed on the substrate by converting selected portions of a photo-definable layer to an insulative material through exposure to electromagnetic radiation in a ~~positive~~ negative mask scheme and by using exposed portions of the photo-definable layer as a mask to form at least one self-aligned contact.

In yet a further embodiment, the present invention is a process for using a photo-definable layer in a Damascene process to create a patterned structure. This process may include forming a photo-definable layer that is convertible to an insulative material, exposing selected portions of the photo-definable layer to electro-magnetic radiation to convert the selected portions to an insulative material, removing non-exposed portions of the photo-definable layer with an etch process to form a desired pattern within the exposed portions of the photo-definable layer, and leaving the exposed portions of the photo-definable layer on the substrate as an insulative layer. In a further embodiment, the present invention is a conductive interconnect structure including a substrate, and a patterned insulative layer on the substrate formed by converting selected portions of a photo-definable layer to an insulative material through exposure to electromagnetic radiation in a ~~positive~~ negative mask scheme, by removing non-exposed portions of the photo-definable layer to form a pattern within the photo-definable layer, and by leaving the exposed portions of the photo-definable layer as the patterned insulative layer. Additionally, this structure may include a conductive layer inlaid within the patterned insulative layer.

In another embodiment, the present invention is a process for using a photo-definable layer in a dual Damascene process to create a patterned structure. This process may include forming a first photo-definable layer that is convertible to an insulative material and exposing selected portions of the first photo-definable layer to electro-magnetic radiation to convert the selected portions to an insulative material to define desired contact areas. The process may also include forming a second photo-definable layer that is convertible to an insulative material, exposing selected portions of the second photo-definable layer to electro-magnetic radiation to convert the selected portions to an insulative material to define a desired interconnect pattern, and removing non-exposed portions of the first and second photo-definable layers to form voids exposing the desired contact areas and the desired interconnect pattern. In a further embodiment, the present invention is a conductive interconnect structure including a substrate, a first conductive layer on the substrate, and a patterned insulative layer on the first conductive layer formed by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a ~~positive~~ negative mask scheme, by removing non-exposed portions of the photo-definable layer to form a pattern within the photo-definable layer, and by leaving the exposed portions of the photo-definable layer as the patterned insulative layer. This structure may further include a second conductive layer inlaid within the insulative layer forming contacts with selected portions of the first conductive layer.

On page 9, the first paragraph:

FIGS. 4a-4~~e~~c show a sequence of three-dimensional structures wherein trenches have been added to a base structure in a Damascene process wherein the photo-definable layer may be left to form an integral part of an oxide layer.

On page 11, the first full paragraph:

Example structures that may be formed and process steps involved are shown in FIGS. 1a-e, 2a-d, 3a-d, 4a-e~~c~~, 5a-e, 6a-f, and 7a-d. These examples utilize plasma polymerized

methylsilane (PPMS) as the material with which to form the photo-definable layer. FIGS. 1a-e, 4a-~~e~~c, 5a-e and 6a-f depict process steps in which exposed PPMSO portions are used as a patterned mask for further processing steps. FIGS. 2a-d, 3a-d and 7a-d depict process steps in which non-exposed PPMS portions are used as a patterned mask for further processing steps. Although these examples use PPMS to form the photo-definable layer, it is understood that other photo-definable layers may be used as desired, with corresponding modifications to process steps depending upon the particular material chosen.

On pages 17-18, in the paragraph beginning at the bottom of page 17:

In contrast to FIGS. 5a-e, the non-exposed portion 673 may be removed using an etch with good selectivity to silicon to create void 675 as shown in FIG. 6c. After the non-exposed portions are removed, a second photo-definable PPMS layer 676 may be formed on top of the first PPMS layer 672 as shown in FIG. 6d. The second PPMS layer 676 may then be irradiated with DUV radiation 670 in the presence of oxygen to convert exposed portions 678 to PPMSO. As with the first layer and as shown in FIG. 6e, portions 677 of the second PPMS layer 676 may be masked from exposure in a negative scheme using well known photo-lithography techniques. An etch with good selectivity to silicon, for example a chlorine or bromine based plasma etch, may now be used to remove the non-exposed portions 677 of the second PPMS layer ~~565~~ 676 to create void 679, as depicted in FIG. 6f. The transformation of the remaining PPMSO portions ~~564~~ 674 and ~~566~~ 678 to silicon oxide may be completed by ashing in oxygen at an elevated temperature, for example at a temperature greater than 200°C, followed by an anneal in oxygen, for example at about 400°C. To complete the dual Damascene process, a metal layer may be deposited filling in the voids left by the removal of portions 674 and 678.

On pages 18-19, replace the paragraph beginning at the bottom of page 18:

The exposed portion 786 of the PPMS layer 783, as well as the photoresist layer ~~785~~ 784, may then be irradiated with DUV radiation 785 in the presence of oxygen as shown in FIG. 7b.

The exposed portion 786 of the PPMS layer 783 will be converted to PPMSO, and the photoresist layer 784 is simultaneously cross-linked and thereby hardened. Alternatively, the cross-linking of the photoresist may occur in a discrete step. Next, an oxide etch that has high selectivity to silicon, for example a chlorine or bromine based plasma etch, may be used to remove the exposed PPMSO portions 786 and the underlying oxide within dielectric layer 781, as depicted by void 787 in FIG. 7c. Any remaining photoresist may then be stripped. The remaining non-exposed PPMS portions 788 may then be converted to PPMSO through exposure to DUV radiation in the presence of oxygen. The conversion of the PPMSO layer to silicon oxide may be completed by ashing in oxygen at an elevated temperature, for example at a temperature greater than 200°C, followed by an anneal in oxygen, for example at about 400°C. In the resulting structure, as shown in FIG. 7d, the PPMS layer has become an integral part of the dielectric layer 781.